DATASHEET

RELEASED 8/16

Hardened-by-Design (HBD) Standard Cell

UT130nHBD

Features

- Up to 15,000,000 usable NAND2 equivalent gates using standard cell architecture
- Toggle rates up to 1.5 GHz
- Advanced 130nm bulk silicon gate CMOS processed in a commercial fab
- Operating voltage 3.3V I/O and 1.2V core
- Multiple product assurance levels available in QML Q and V, military and industrial
- Radiation hardened from 100 krad(Si) to 300 krad(Si) total dose available using CAES Colorado Springs's (CAES) RadHard-by-Design techniques
- SEU-immune to less than $1.0x10^{-10}$ errors/bits-day available using special library cells
- Special I/O offering: HSTL, Class I and II, LVDS
- Robust CAES Design Library of cells and macros
- Support for Verilog and VHDL design languages on Linux workstations
- Cell models validated in Mentor Graphics® and Synopsys™ design environments
- Full complement of industry standard IP cores
- Wide selection of SP/DP SRAMs with optional MBIST and EDAC
- Low power dissipation of 18nW/MHz/gate at 1.2V VDDQ
- Operating temperature range of -55°C to +125°C
- Package pin count of up to 624 for wire bond and 1248 for Flip-Chip (in development)

Product Description

CAES high performance UT130nHBD Hardened-by-Design ASIC standard cell family features densities up to 15,000,000 NAND2 equivalent gates and will be available in multiple quality assurance levels such as MIL-PRF-38535, QML V and Q, military, industrial grades and non-RadHard versions.

For those designs requiring stringent radiation hardness, CAES 130nm process employs a special technique that enhances the total dose radiation hardness to 300 krad(Si) while maintaining circuit density and reliability. In addition, the process uses epitaxial wafers for greater transient radiation hardness and latch-up immunity.

The UT130nHBD ASIC family uses highly efficient standard cell architecture for internal cell instantiation developed using CAES patented architectures. Combined with state-of-the-art, timing driven placement and routing tools, the area utilization and signal routing of transistors is maximized using six metal interconnect routing layers. Table 1, 2 and 3 summarizes some of the most important aspects of the 130nm ASIC Library.

The UT130nHBD ASIC family is supported by an extensive cell library that includes standard logic functions, Phase Lock Loop (PLL) and SRAM with optional MBIST and EDAC. CAES IP library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- CAES IP

We offer CAES LEON3 and RTL based IP.

Table 1: Library Overview

Charactristics	Value
Technology	TSMC 130G - 130nm Bulk CMOS, 8 metal layers
Logic Density	86K gates/mm2 = ~15M gates
Supply Voltages	3.3V; 1.2V core
Typical Power Dissipation	~ 18nW/gate-MHz @ 1.2V
Standard Cells	~ 300 multi-VT cells (high VT, standard VT and low VT)
Intrinsic Gate Delay (na02nd2)	50ps
Fastest Core Frequency	570 MHz (10 levels of logic)
I/O's	3.3V; 4, 8, 12, 24mA outputs; LVCMOS, LVTTL, Schmitt trigger; bidirectional, programmable, configurable pull up/down
Memories	Single & Dual-port SRAM & Register file compiler
Macros	HSTL (250MHz), LVDS (400Mbps), PLL's (100-500MHz), SerDes(3.125Gbps - in development)
Rated Temp Range	-55°C to 125°C
ESD (Human Body Model)	1kV
Packaging Options	Wirebond: CQFP, CCGA, CBGA. Flip Chip (in development)

Absolute Maximum Ratings [1]

(All supplies referenced to ground)

Symbol	Parameter	Limits
V_{DDIO} [2]	I/O DC supply voltage	-0.3V to 3.3V +30%
V_{DDQ} [2]	Core DC supply voltage	-0.3V to 1.2V + 30%
T_{STG}	Storage temperature	-65°C to +150°C
T_J	Maximum junction temperature	+150°C
I_{LU}	Latchup immunity	±150mA
I_I	DC input current	±10mA
T_{LS}	Lead temperature (soldering 5 sec)	+300°C

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) The recommended "power-on" sequences is VDDQ voltage supply applied first, followed by the VDDIO voltage supply. The recommended "power-off" sequence is the reverse. Remove VDDIO voltage supply, followed by removing VDDQ voltage supply.

Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DDIO}	IO DC supply voltage	3.0V ± 0.3
V_{DDQ}	Core DC supply voltage	1.2V± 0.1

Low-Noise Device and Package Solutions

Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, CAES offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes (Table 2). These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 352 leads. PGAs are available with up to 299 pins and LGAs/CCGAs up to 624 pins. CAES flat-packs feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations.

In addition to the packages listed in Table 2,CAES offers custom package development and package tooling modification services for individual requirements. For ASIC's that require high signal I/O count, CAES has flip chip packaging solutions.

Table 2: Packaging

Type	Total Pins
Flatpack	Up to 352
PGA	299
LGA [4]	472,624

Notes:

1) Contact CAES for specific package drawings.
2) External chip capacitor attachment available to space quality levels (for improved SSO response).
3) CAES supports all JEDEC outline package designs.
4) LGA package formats can be provided with Solder Columns.

Extensive Cell Library

The UT130nHBD ASIC family is supported by an extensive cell library that includes standard logic functions, Phase Lock Loop (PLL) and SRAM with optional MBIST and EDAC. User-selectable options for cell configurations include scan and radiation hardness (SEU) levels for all register elements, as well as output drive strength.

Phase-Locked Loop (PLL) macro cell is derived from the SerDes PLL and is capable of covering a frequency range of 100MHz to 500MHz. The PLL supports a power-down mode and phase lock indicator.

Refer to CAES UT130nHBD Design Manual for complete cell listing and details.

I/O Buffers

The UT130nHBD family offers a high number of specialized I/O's. For any specific design, signal availability is affected by package selection and IO type. The LVCMOS I/O cells can be configured by the user to serve as input, output, bidirectional or three-state. Output drive options range from 4, 8, 12 and 24mA. To drive larger off-chip loads output drivers may be combined in parallel to provide additional drive up to 48mA.

Other I/O buffer features and options include:

- Internally Configurable weak pull-up and pull-down devices
- Schmitt trigger
- LVDS
- HSTL

LVDS transmitter (Tx) and receiver (Rx) buffers are enhanced versions of the CAES Standard Products UT54LVDS031LV LVDS driver and UT54LVDS032LV receiver products. They provide the same >400Mbps (200MHz) switching rates, 340mV nominal differential signaling levels, transmitter enable and receiver fail-safe circuitry. Each supports a power-down mode that configures the I/O buffers into their lowest power state. A unique CAES reference circuit improves performance matching between multiple Tx buffers and multiple Rx buffers.

CAES ASIC HSTL bidirect, tristate and input buffers are based on the EIA/JEDEC Standard EIA/JESD8-6 (August 1995) Class-1 and -2. They provide switching rates of 250MHz and all support a power-down mode.

JTAG Boundary-Scan

The UT130nHBD family allows for insertion of a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits of this capability are:

- Easy test of complex assembled printed circuit boards
- Gain access to and control of internal scan paths
- Initiation of Built-In Self Test

Clock Driver Distribution

CAES design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

CAES specializes in high-performance circuits designed to operate in harsh military and radiation environments.

Typically the propagation delay for a CMOS device is a function of its fanout loading, input slew, supply voltage, operating temperature and processing radiation tolerance. In a radiation environment additional performance variances must be considered.

The UT130nHBD simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Power consumption of internal gates and I/O buffers is based on many factors including switching frequency, loading, voltage, temperature and transistor leakage characteristics. CAES radiation-tolerant process exhibits power dissipation that is typical of commercial CMOS processes. The UT130nHBD cell library supports a low power design methodology by providing high threshold voltage VT versions of the core cells to reduce leakage current. Additionally the library contains clock gating cells that can be used to reduce switching activity in designs. For rigorous power estimation methodology refer to the CAES UT130nHBD Design manual or consult with a CAES Applications Engineer.

ASIC Design Software

Using a combination of state-of-the-art third-party and proprietary design tools CAES delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

CAES flexible circuit creation methodology supports high level design methodology by providing synthesis libraries in Liberty syntax. Compiled technology files are provided for Synopsys synthesis and design analysis tools. Design verification is performed in any VHDL or Verilog simulation environment using CAES robust libraries. CAES also supports Automatic Test Program Generation and Memory BIST to improve design testing.

CAES HDL Design Systems

CAES offers a Hardware Description Language (HDL) design system supporting both VHDL and Verilog that allows easy access to CAES RadHard capabilities. Both the VHDL and Verilog libraries provide sign-off quality models and robust tools.

The VHDL libraries are VITAL 3.0 compliant and the Verilog libraries are OVI 1.0 compliant. With the library capabilities CAES provides, you can use High Level Design methods to synthesize your design for simulation. CAES also provides tools to verify that your HDL design will result in successful implementations.

CAES PIONEERING ADVANCED ELECTRONICS
4350 Centennial Blvd. | Colorado Springs CO 80907 USA | 1-800-645-8862 | cobhamaes.com

Hardened-by-Design (HBD) Standard Cell

UT130nHBD

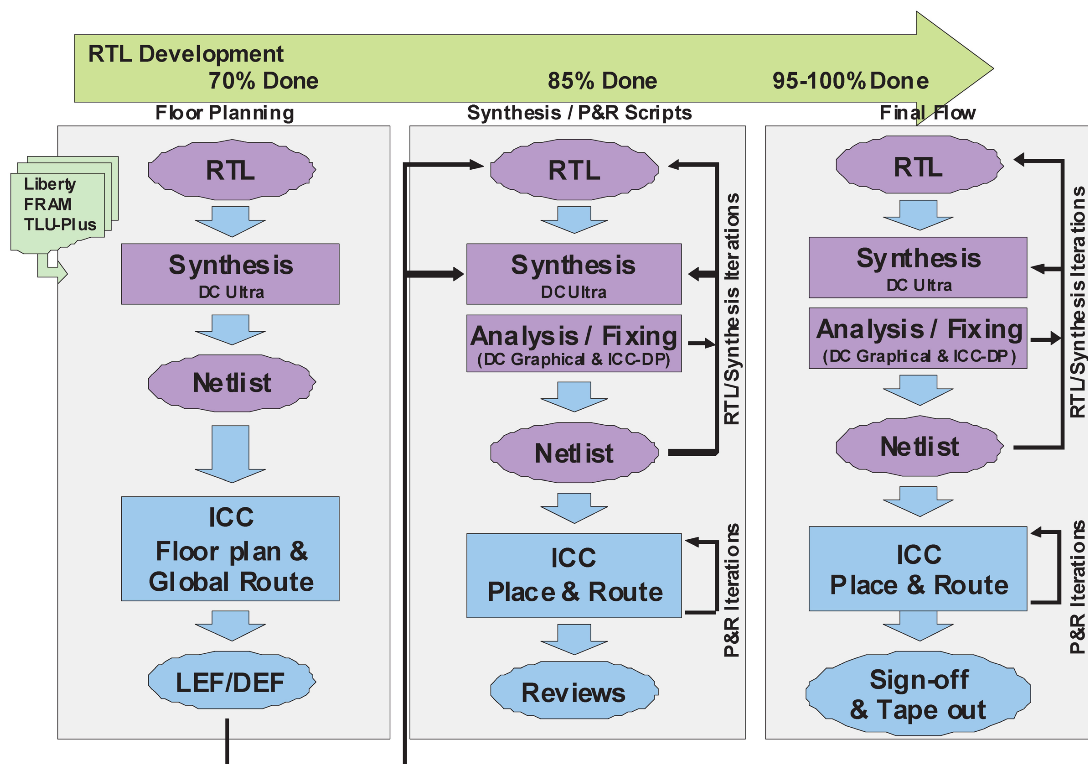

Figure 1: Design Plan

Advantages of the CAES HDL Design Systems

- The CAES HDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence and other vendors to help you synthesize and verify a design.
- CAES Logic Rules Checker and Tester Rules Checker allow you to verify partial or complete designs for compliance with CAES design rules.
- CAES HDL Design System accepts back-annotation of timing information through SDF.

XDT℠ (External Design Translation)

Through CAES XDT services, customers can convert an existing non-CAES design to CAES UT130nHBD platform for increased power/speed performance. The XDT capability is particularly useful for converting an FPGA to CAES radiation-tolerant technology. The XDT translation tools convert industry standard netlist formats and 3rd party vendor libraries to CAES formats and libraries. Industry standard netlist formats supported by CAES include:

- VHDL
- Verilog HDL
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

Hardened-by-Design (HBD) Standard Cell

UT130nHBD

Tools Supported by CAES

CAES supports libraries for:

- Mentor Graphics
  - QuestaSim
  - Tessent FastScan
  - Tessent MBIST
- Synopsys
  - Design Compiler (with PowerCompiler)/Ultra
  - PrimeTime
  - PrimePower
  - VCS for Verilog and VHDL
  - Formality
  - TetraMax
- VITAL-compliant VHDL Simulation Tools
- OVI-compliant Verilog Simulation Tools

Training and Support

CAES personnel conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

Physical Design

By using five layers of metal interconnect CAES achieves optimized layouts that maximize speed of critical nets, overall chip performance and design density up to 15,000,000 NAND2 equivalent gates.

Test Capability

CAES supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation and fault grading. Serial scan design options are available on all UT130nHBD storage elements. Automatic test program development capabilities handle large vector sets for use with CAES Teradyne Tiger ATE's, supporting high-speed testing (up to 1.2GHz).

Quality and Reliability

CAES is dedicated to meeting the stringent performance requirements of aerospace and defense systems suppliers. CAES maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO- 9001. In 1988 we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). CAES utilizes the wafer foundry's data from TCV test structures to evaluate hot carrier aging, electromigration and time dependent test samples for reliability testing.

Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

Radiation Tolerance

CAES incorporates radiation-tolerance techniques in process design, design rules, array design, power distribution and library element design. All key radiation-tolerance process parameters are controlled and monitored using statistical methods and in-line testing (Table 3).

Table 3: Radiation Hardness

Parameter	Radiation Tolerance	Notes
Total ionizing dose	100-300 krad(Si)	1,2
Single event upset (SEU)	$<1.0\times10^{-10}$ errors per cell-day	3,4
Single event latchup (SEL)	Latchup immune to LET = 115 MeV/cm2/mg	5

Notes:

1) Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019.
2) TID data measured at 1.35V core/3.6V I/ O VDDIO. All post radiation values measured at 25°C.
3) SEU limit based on standard evaluation circuit at 1.1V core/3.0V I/ O VDDIO 25°C condition.
4) SEU-hard flip-flop cell. Non-hard flip-flop typical is 5x10-8.
5) SEL data measured at 1.3V core/3.6V I/ O VDDIO and 125°C.

Intel is a registered trademark of Intel Corporation
Mentor, Mentor Graphics, AutoLogic II, QuickSim II, QuaickFault II, QuickGrade II, FastScan, FlexTest, QuestaSim and DFT Advisor are registered trademarks of Mentor Graphics Corporation
Verilog and Leapfrog are registered trademarks of Cadence Design Systems, Inc.
Synopsys, Design Compiler, Test Compiler Plus, VHDL Compiler, Verilog HDL Compiler, TestSim and VSS are trademarks of Synopsys, Inc.

Data Sheet Revision History

REV	Revision Date	Description of Change	Page(s)
A	8-22-16	Added CAES data sheet template. Removed Sun Design Support. Removed Mentor ModelSim tools and replaced with QuestaSim	All 1 7

UT130nHBD

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

RELEASED 8/16

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

Cobham Colorado Springs Inc. d/b/a Cobham Advanced Electronic Solutions (CAES) reserves the right to make changes to any products and services described herein at any time without notice. Consult an authorized sales representative to verify that the information in this data sheet is current before using this product. The company does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing; nor does the purchase, lease, or use of a product or service convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of the company or of third parties.