DATASHEET

RELEASED 7/31/20

Voltage Supervisor

UT04VS50P

Features

- 4.5V to 5.5V Operating voltage range.
- 6 Fixed Threshold Voltage Monitors (3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1.0V)
- Fixed & Adjustable Threshold Voltage Select modes
- Threshold Voltage Select with TH0, TH1 pins
- Adjustable RESET Timeout with external capacitor
- Independent Voltage Monitoring and Sequencing
- Manual Reset Input Pin
- Active Low and Active High RESET pins
- Output Voltages Open Drain
- Two VOUTS active high and two VOUTS programmable with INV Pin
- RESET, RESETB Outputs Open Drain
- Over-voltage Detection Mode
- Operating Temperature Range -55°C to +125°C
- Low Power Typical 1000µA
- Tolerance Select Input Pin (5% & 10%)
- RESET, RESETB, VOUT1, VOUT2, VOUT3 and VOUT4 guaranteed to be in the correct state for V_{DD} down to 1.2V
- Packaging options:
  - Total dose: 300 krad(Si)
- Operational environment:
  - Total dose: 300 krad(Si)
    - SEL Immune: ≤110 MeV-cm^2/mg @125°C
    - SEL Immune: ≤109MeV-cm^2/mg
- Standard Microelectronics Drawing (SMD) 5962-13206
  - QML Q and V

Introduction

The UT04VS50P is a radiation-hardened Voltage Supervisor which simultaneously monitors up to four supply levels utilized in a system, providing status output for each signal, VOUTx, as well as system reset signal if any of the monitored signals moves out of range. To set the monitor trip points, the TH0 and TH1 pins allow the selection of three sets of preset threshold levels per channel, determined by an internal bandgap voltage reference, to reduce supply and temperature variance. A fourth selection allows the user to determine the level for each channel. There are two modes of operation, determined by the OVSH pin. In the first mode, when the OVSH pin is connected to V_{SS}, four independent supplies are monitored for an under-voltage condition. In the second mode when the OVSH pin is connected to V_{DD}, under-voltage and over- voltage of the inputs are monitored. In this mode, two supplies can be monitored using channels 1 and 3 or channels 2 and 4, respectively. For flexibility, both system RESET and RESETB outputs are available for interfacing to the system. Each channel has an enable, ENx, allowing use of one, two, three or all four monitor channels.

This device includes a 3V regulator that supplies power to the internal circuitry. The margin (or tolerance) to the given threshold voltage, for under-voltage monitoring, is determined by the setting of the TOL pin. The logic sense of the channel 3 and 4 outputs can be inverted by setting the INV pin, appropriately. Also, MRB, master reset, provides a means for a manual input to activate the RESET signals. In addition, the user can adjust two timing parameters by the addition of external capacitors to the device. These are the response times of the channel VOUTx signal when the associated input returns to a valid level, implemented by a capacitor connected to CDLYx and the time to clear RESET (and RESETB) when a channel enable or input level becomes valid; implemented by CRESET.

Voltage Supervisor

UT04VS50P

Application

The UT04VS50P supervisory circuit reduces the complexity and number of circuits required to monitor power supply and battery functions in microprocessor, DSP, microcontroller, ASIC and FPGA systems. The UT04VS50P supervisory circuit significantly improves system reliability and accuracy over comparable systems that use separate ICs or discrete components.

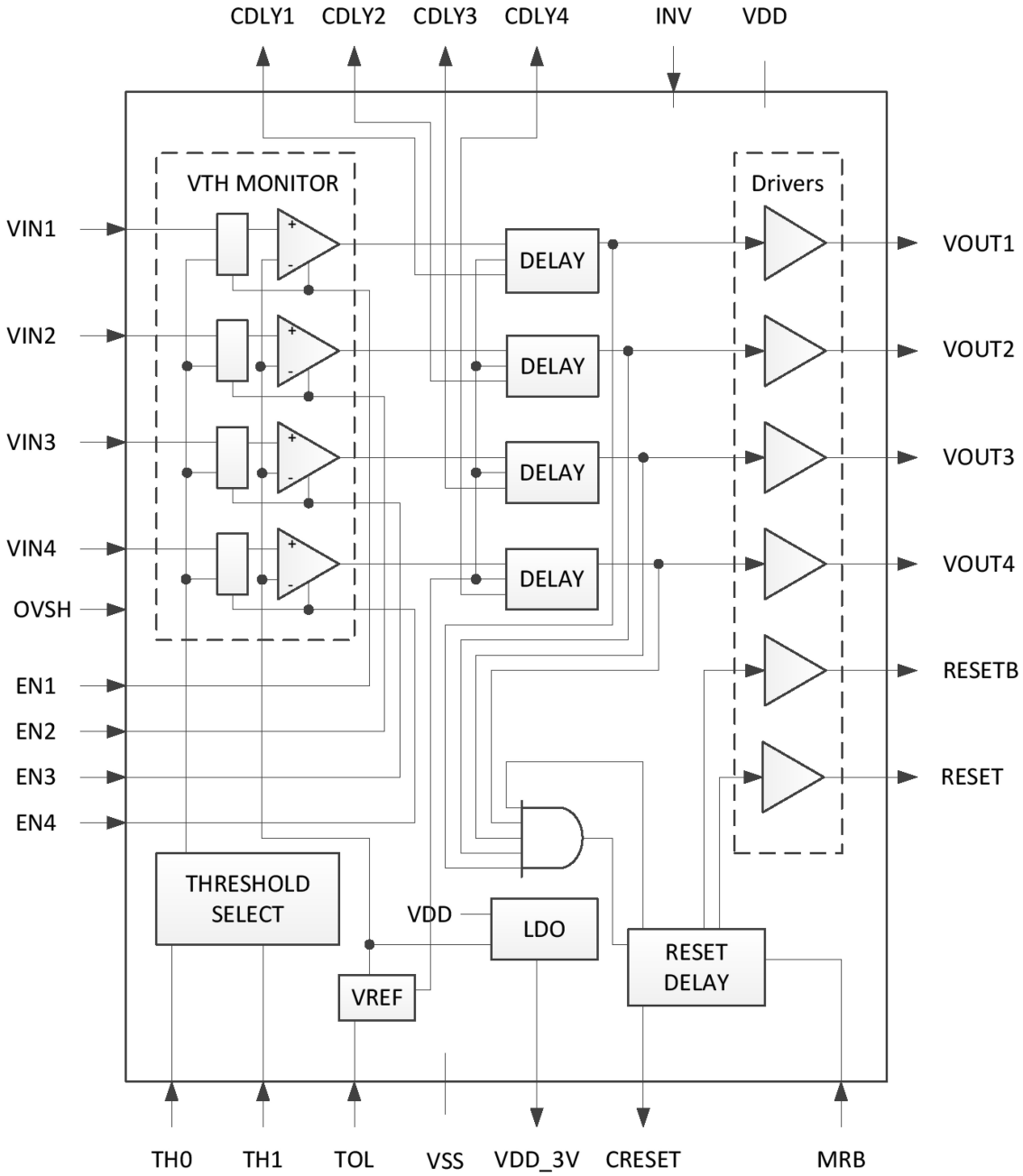


Figure 1. UT04VS50P Block Diagram

Voltage Supervisor

UT04VS50P

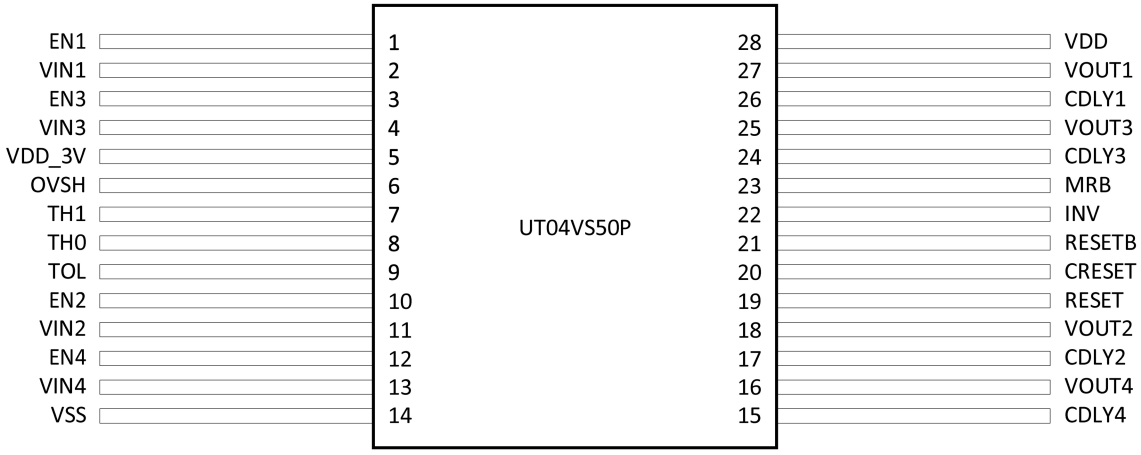


Figure 2. UT04VS50P Pin Configuration

Pin Descriptions

Number	Pins	Type	Description
1	EN1	Digital Input	Active high enable for VIN1. Setting this pin low forces VOUT1 low regardless of the value of VIN1. Setting this pin high enables the monitor circuitry for VIN1.
2	VIN1	Analog Input	Analog input VIN1. When enabled the voltage input is monitored for an under-voltage condition; see Functional Descriptions - Thresholds, Over-voltage Setting/Tolerance. The condition is output on VOUT1.
3	EN3	Digital Input	Active high enable for VIN3. Setting this pin low forces VOUT3 low when OVSH=0 (VOUT3 is forced low when OVSH=1) regardless of the value of VIN3. Setting this pin high enables the monitor circuitry for VIN3.
4	VIN3	Analog Input	Analog input VIN3. When enabled and dependent on the mode of operation (OVSH), the voltage input is monitored for an under-voltage or over-voltage condition; see Functional Descriptions - Thresholds, Over-voltage Setting/Tolerance. The condition is output on VOUT3 when OVSH=0 and on VOUT1 when OVSH=1.
5	VDD_3V	3V Regulated Supply	3V internal regulator output voltage. (See functional description - 3V regulator). This is an internal voltage reference only. It is not provided as a regulated voltage for external use. This pin requires external bypass capacitors to chip ground VSS.
6	OVSH	Digital Input	Over-voltage pin. When OVSH = 1, the over-voltage mode is enabled. This allows for the monitoring of both over-voltage and under-voltage of two supplies. Inputs VIN1 and VIN2 function normally, while VIN3 is used to monitor an over-voltage condition in conjunction with the VIN1 source and VIN4 likewise for the VIN2 source. See Functional Descriptions - Thresholds, Over-voltage Setting/Tolerance. When OVSH=0 all four inputs, VIN1, VIN2, VIN3 and VIN4 monitor under- voltage.

Voltage Supervisor

UT04VS50P

Pin Descriptions (Continue)

Number	Pins	Type	Description
7	TH1	Digital Input	Digital Threshold select1. Used with TH0 to select one of four analog input voltage thresholds. (See Table 2)
8	TH0	Digital Input	Digital Threshold select0. Used with TH1 to select one of four analog input voltage thresholds. (See Table 2)
9	TOL	Digital Input	Threshold tolerance select sets the accuracy of the threshold to 5% below the nominal value by connecting TOL to logic 0. Connecting TOL to logic 1 sets the threshold voltage to 10% below the nominal value.
10	EN2	Digital Input	Active high enable for VIN2. Setting this pin low forces VOUT2 low regardless of the value of VIN2. Setting this pin high enables the monitor circuitry for VIN2.
11	VIN2	Analog Input	Analog input VIN2. When enabled, the voltage input is monitored for an under-voltage condition; see Functional Descriptions - Thresholds, Over-voltage Setting/Tolerance. The condition is output on VOUT2.
12	EN4	Digital Input	Active high enable for VIN4. Setting this pin low forces VOUT4 low when OVSH=0 (VOUT4 is forced low when OVSH=1) regardless of the value of VIN4. Setting this pin high enables the monitor circuitry for VIN4.
13	VIN4	Analog Input	Analog input VIN4. When enabled and dependent on the mode of operation (OVSH), the voltage input is monitored for an under-voltage or over-voltage condition; see Functional Descriptions - Thresholds, Over-voltage Setting/Tolerance. The condition is output on VOUT4 when OVSH=0 and on VOUT2 when OVSH=1.
14	VSS	Supply GND	Ground. This pin must be tied to system ground to establish a reference for voltage detection.
15	CDLY4	Analog Output	External capacitor delay connection. Allows adjustment of the VOUT4 timing after VIN4 becomes valid, when OVSH = 0. See Functional Descriptions - CDLY timing section.
16	VOUT4	Open Drain Digital Output	Output of VIN4 monitor when OVSH = 0; inactive when OVSH=1. With INV=0, logic 1 indicates that the VIN4 input is at a valid level. With INV=1, logic 0 indicates that VIN4 is at a valid level. Device contains active pull-down device; requires external pull-up.
17	CDLY2	Analog Output	External capacitor delay connection. Allows adjustment of the VOUT2 timing after VIN2 becomes valid. See Functional Descriptions - CDLY timing section.
18	VOUT2	Open Drain Digital Output	When OVSH=0, it indicates the signal state of the VIN2 monitor. When OVSH=1, it indicates the combined signal states for VIN2 and VIN4 (under-voltage and over-voltage detection). See Functional Descriptions - Thresholds, Device contains active pull-down device; requires external pull-up.

Voltage Supervisor

UT04VS50P

Pin Descriptions (Continue)

Number	Pins	Type	Description
19	RESET	Open Drain Digital Output	Active high output indicating a system reset condition is activated by appropriate condition on VOUTx, ENx, or MRB pin. See discussion for state changes and timing information. Device contains active pull-down device; requires external pull-up.
20	CRESET	Analog Output	External capacitor delay connection. Allows adjustment of RESET timeout, which is the time RESET is held after all reset input conditions are cleared. See Functional Description - CRESET timing section.
21	RESETB	Open Drain Digital Output	Active low output indicating a system reset condition is activated by appropriate condition on VOUTx, ENx, or MRB pin. See discussion for state changes and timing information. Device contains active pull- down device; requires external pull-up.
22	INV	Digital Input	When logic 1, inverts the sense of the VOUT3 and VOUT4 outputs.
23	MRB	Digital Input Internal Pull-up	Master Reset active low input. This forces the RESET/RESETB pins to their active state. See discussion for timing information.
24	CDLY3	Analog Output	External capacitor delay connection. Allows adjustment of the VOUT3 timing after VIN3 becomes valid when OVSH=0. See Functional Descriptions - CDLY timing section.
25	VOUT3	Open Drain Digital Output	Output of VIN3 monitor when OVSH=0; inactive when OVSH=1. With INV=0, logic 1 indicates that the VIN3 input is at a valid level. With INV=1, logic 0 indicates that VIN3 is at a valid level. Device contains active pull-down device; requires external pull-up.
26	CDLY1	Analog Output	External capacitor delay connection. Allows adjustment of the VOUT1 timing after VIN1 becomes valid. See Functional Descriptions - CDLY timing section.
27	VOUT1	Open Drain Digital Output	When OVSH=0, it indicates the signal state of the VIN1 monitor. When OVSH=1, it indicates the combined signal states for VIN1 and VIN3 (under-voltage and over-voltage detection). See Functional Descriptions - Thresholds, Device contains active pull-down device; requires external pull-up.
28	VDD	Supply	Supply voltage, 4.5 to 5.5V.

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID) [1]	300	krad(Si)
Single Event Latchup Immune (SEL) [2]	≤110	MeV-cm²/mg
Single Event Transient Immune (SET)	≤109	MeV-cm²/mg

Voltage Supervisor

UT04VS50P

Notes:

1) Using MIL-STD-883, TM1019, Condition A.
2) Worst case temperature and voltage of Tc = +125°C, VDD = 5.5V.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limits	Units
V_{DD}	Positive supply voltage	7.2	V
V_{IO}	Voltage on any I/O pin	-0.3 to V_{DD} + 0.3V	V
I_{IO}	DC I/O current	±10	mA
P_D	Power dissipation	1.0	W
Θ_{JC}	Thermal resistance, junction to case	16	°C/W
T_{LEAD}	Lead temperature (soldering 10 seconds)	300	°C
T_J	Maximum junction temperature	+175	°C
T_{STOR}	Storage temperature	-65 to +150	°C
V_{ESD}	ESD_{HBM}	1000	V

Note:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Positive supply voltage	4.5 to 5.5	V
V_{SS}	Negative supply voltage	0.0	V
T_C	Case temperature range	-55 to +125	°C
V_{IN}	Analog inputs Digital inputs	0.6 to 3.6 V_{SS} to V_{DD}	V

Voltage Supervisor

UT04VS50P

DC Electrical Characteristics [1,2]

(V_{DD}=4.5V to 5.5V; -55°C ≤ TC ≤ +125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
Power Supply					
I_{DD}	V_{DD} supply current	All V_{OUTX} high		1250	µA
Digital Inputs and Outputs					
V_{IL}	Digital input low		-0.3	0.3*V_{DD}	V
V_{IH}	Digital input high		0.7*V_{DD}	V_{DD}+0.3	V
V_{ILMRB}	MRB Digital input low		-0.3	0.8	V
V_{IHMRB}	MRB Digital input high		2.0	V_{DD}+0.3	V
$V_{HYSTMRB}$	MRB Input voltage hysteresis		60		mV
I_{MRB}	MRB pull-up current	MRB=0V V_{DD}=5.5V for Max I_{MRB}		330	µA
V_{OL}	Open drain digital output low	V_{DD} =5.5V I sink=1mA		0.3	V
I_{CH_RESET} [3]	Charge current CRESET	V_{DD} =5.0V	0.35	1.25	µA
I_{OZL}	Digital output leakage current low		-1	1	µA
I_{OZH}	Digital output leakage current high		-1	1	µA
I_{IL}	Digital input leakage current low		-1	1	µA
I_{IH}	Digital input leakage current high		-1	1	µA
I_{CH_CDLY} [3]	Charge current CDLY	V_{DD}=5.0V	0.55	1.9	µA
V_{TH_CDLY} [3]	Threshold CDLYx	CDLY rising	1.17	1.23	V
$V_{TH\_CRESE_T^3}$	Threshold CRESET	CRESET rising	1.17	1.23	V
V_{RFTH}[3]	Reference threshold voltage		585	615	mV
Analog Inputs					
V_{TH_VIN}	Analog threshold under-voltage case	3.3V threshold, TOL= 0	2.97	3.135	V
		3.3V threshold, TOL= 1	2.805	2.970	V
		2.5V threshold, TOL= 0	2.25	2.375	V
		2.5V threshold, TOL= 1	2.125	2.250	V
		1.8V threshold, TOL= 0	1.620	1.710	V
		1.8V threshold, TOL= 1	1.530	1.620	V
		1.5V threshold, TOL= 0	1.350	1.425	V
		1.5V threshold, TOL= 1	1.275	1.350	V
		1.2V threshold, TOL= 0	1.080	1.140	V
		1.2V threshold, TOL= 1	1.020	1.080	V
		1.0V threshold, TOL= 0	0.90	0.950	V
		1.0V threshold, TOL= 1	0.85	0.915	V
C_{VINX} [3]	VINx input capacitance			15	pF

ENx	INV	VINx	VOUT1-2	VOUT3-4
0	0	$V_{INx}<V_{TH\_VIN}$	0	0
1	0	$V_{INx}<V_{TH\_VIN}$	0	0
0	0	$V_{INx}>V_{TH\_VIN}$	0	0
1	0	$V_{INx}>V_{TH\_VIN}$	1	1
0	1	$V_{INx}<V_{TH\_VIN}$	0	1
1	1	$V_{INx}<V_{TH\_VIN}$	0	1
0	1	$V_{INx}>V_{TH\_VIN}$	0	1
1	1	$V_{INx}>V_{TH\_VIN}$	1	0

Notes:

1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is specified at 25°C per MIL-STD-883 Method 1019, Condition A, up to the maximum TID level procured (see ordering information).
2) RESET, RESETB, VOUT1, VOUT2, VOUT3 and VOUT4 guaranteed to be in the correct state for V_{DD} down to 1.2V.
3) Guaranteed by design but not tested.

AC Characteristics Read Cycle (Post-Radiation) *

(V_{DD} = 4.5V to 5.5V; -55°C < T_C < +125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
t_{DELAY+} [1]	V_{IN}+ to V_{OUT} propagation delay	V_{IN} rising, CDLY open	11	60	µs
t_{DELAY+}	V_{IN}+ to V_{OUT} propagation delay	V_{IN} rising, Cdly capacitance value on CDLYx=112pF (Figure 3, Test Circuit Load)	81	263	µs
t_{DELAY-}	V_{IN}- to V_{OUT} propagation delay	V_{IN} falling		40	µs
t_{RP} [1]	Reset timeout period	CRESET open	42	158	µs
t_{RP}	Reset timeout period	Creset capacitance value on CRESET=65pF (Figure 3, Test Circuit Load)	103	387	µs
t_{ON} [1]	EN+ to V_{OUT} propagation delay	EN rising to V_{OUT} going high CDLY open	11	60	µs
t_{ON}	EN+ to V_{OUT} propagation delay	EN rising to V_{OUT} going high, Cdly capacitance value onCDLYx=112PF (Figure 3, Test Circuit Load)	81	263	µs
t_{OFF}	EN- to V_{OUT} propagation delay	EN falling to V_{OUT} deasserted		4	µs
t_{MRST}	MRB- to RESET/RESETB propagation delay	MRB falling to RESET/RESETB asserted		5	µs
t_{MPW}	Minimum MRB Input pulse width		2.5		µs
t_{MRP}	MRB+ to RESET/RESETB propagation delay	MRB rising to RESET/RESETB deasserted		3	µs
t_{RST_DELAY}	VINx- to RESET/RESETB asserted	V_{IN} falling		40	µs
t_{GLITCH}	ENx or MRB glitch rejection			270	ns
t_{GLITCH_VINx} [1]	VINx glitch rejection			800	ns
t_{R_VDD} [2,3]	V_{DD} rise time power-up			80	ms

Notes:
*Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 300 krad(Si).
1) Guaranteed by design but not tested.
2) VDD power-up voltage ramp is monotonic.
3) Measured from VDD =0V to VDD =5.0V

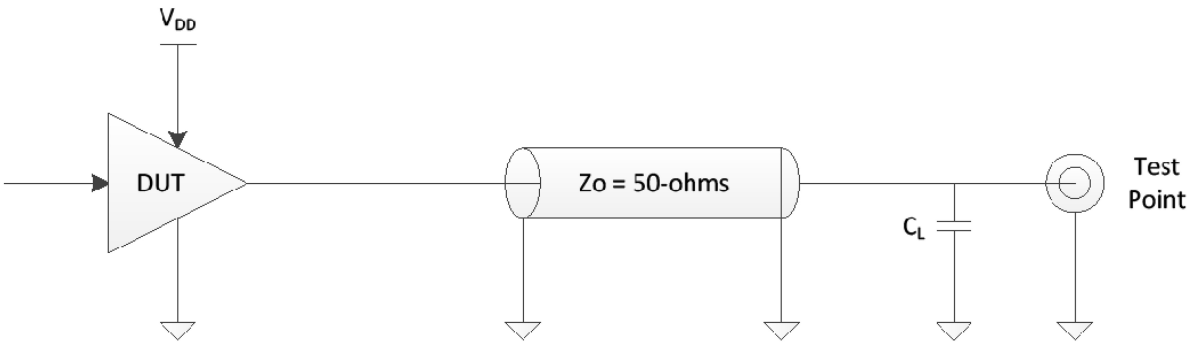


Figure 3: Test Circuit Load used for AC timing

Functional Descriptions

Voltage Inputs

Monitoring of supply levels is done at the VINx pins. Based on the mode of operation (TH0, TH1, OVSH state), the monitored voltage is connected directly to the pin or via a resistive divider. These connections are described further in the Determining a Channel Detection Threshold section.

Resets

The (RESET and RSETB) outputs respond to changes in the state of the enabled channels (either an ENx signal going to the enabled state or a VOUTx signal, of an enabled channel, changing state) and to changes in the master, MRB pin. Timing values are given in the AC Characteristics table and in Figures 4, 5 and 6. These pins are digital output open drain having an active pull-down device, with drive information given in the DC Characteristics table.

Outputs

The VOUTx pins indicate the state of the corresponding supply monitor input source. When the input level is in a valid region, based on the mode and threshold settings, the VOUTx pin is in the logic 1 state. If the channel is disabled or the input level is invalid, the VOUTx pin is in the logic 0 state. In addition, when in over-voltage detect mode (OVSH=1), VOUT3 and VOUT4 are inactive. The INV function, when set to logic 1, inverts the sense of the VOUT3 and VOUT4 pins. There are several timing parameters associated with the state transitions which are described in the Determining a Channel Detection Threshold section. Values for drive and timing are in the DC and AC Characteristics tables.

3V Regulator

The VDD_3V output is generated on-chip by the 3V regulator. It must be bypassed to Vssa with 1.0uF and 0.1uF+/-20% capacitors. See the applications section for further examples. This pin is not intended to supply current for external use. Caution should be exercised with respect to load level leakage currents.

Thresholds/Over-Voltage Setting/Tolerance

Thresholds are determined by several pin settings, TH0, TH1, OVSH and TOL. The variations in operation and setup of the channel inputs, including external components, are described below. The setting of the OVSH pin determines the threshold detection mode for the four channels. When logic 0, all four channels sense when the corresponding input falls below the associated threshold, the under-voltage condition (see Determining a Channel Detection Threshold). In this mode when the signal level falls below the threshold, the corresponding VOUT is switched to logic 0, after a fixed time delay. When the signal returns to a level above the threshold and after the default or user defined delay, (see the CDLY timing section), the VOUT output is switched to the logic 1 state, indicating a valid level (see Figure 6).

For the mode when OVSH is logic 1, over- and under-voltage detection, the input threshold for channels 1 and 2 are handled in the same fashion as for the previously described mode. In this mode, the channel 3 and 4 inputs are checked for an over-voltage condition in conjunction with the voltage monitored on channel 1 and channel 2, respectively. Also, threshold levels are determined differently, see the section on Determining a Channel Detection Threshold and Tables 1A and 1B. The under- voltage condition from channel 1 and the over-voltage condition detected by channel 3 are combined to indicate the occurrence of either condition at the channel 1 output. Likewise, conditions for channel 2 and 4 are combined and indicated at the channel 2 output. **Note:** When OVSH is logic 1, disabling channel 1 or 3 forces VOUT1 to logic 0. The same is true for VOUT2, with respect to the enables for channels 2 and 4. However, only CDLY1 and CDLY2, respectively, are utilized for output timing.

Determining Channel Detection Threshold

For the case of under-voltage sensing utilizing the preset thresholds (TH1 and TH0 both not being logic 1), the actual threshold is based on the nominal threshold levels as shown in Table 2. The actual threshold voltage, accounting for tolerance, based on the TOL pin setting and circuit variations, is given by the following equation (values also listed in the DC Characteristics table):

Vth_actual(nom) =

Vthresh_nominal * [1 - 5% *(1 + TOL) - 2.5%]

where Vthresh-nominal is given in Table 2, TOL is 0 when logic 0 and 1 when logic 1, and 2.5% accounts for circuit variances.

For adjustable under-voltage thresholds, when TH0 = TH1 = logic 1, and over-voltage sensing on the channel 3 and 4 inputs when OVSH = logic 1, the over-voltage (Vth_adj-overV) thresholds are determined by user-implemented resistive dividers placed at the input to the given channel. These threshold levels are determined by the following equation:

Vth_adj-overV = [(RT + RB)/RB +/- 2.5%] * V_{RFTH}

where RT is the top resistor of the divider and RB is the lower resistor tied to VSS, 2.5% accounts for circuit variances and V_{RFTH} is an internally-generated reference voltage. A voltage with value as given in the DC Characteristics table. **Note**: The TOL pin function is not applicable in these modes. In addition to the 2.5% added to account for circuit variations, the user should consider resistor and supply variation tolerances when calculating the values for the resistive divider. Other considerations for the choice of resistor values are power consumption and time delay impact. The nominal capacitance of the input channel is given in the DC Characteristics table.

Note: The maximum level at any analog channel input is limited to 3.6V. This limits the maximum voltage level of the monitored signal. When the device is placed in the adjustable threshold state (TH0 = TH1 = logic 1) utilizing an external resistive divider, the maximum voltage of the monitored signal can be greater than the maximum level when using the preset threshold, as given by:

$Vmonitor < [(RT + RB)/RB] * V_{RFTH}$

where RT is the top resistor of the divider and RB is the lower resistor, tied to VSS. One should account for resistor tolerances. Also, with the resistive divider tied to VSS, the minimum voltage that can be monitored is VRFTH. It is possible to tie the resistive divider to the VDD supply and, hence, monitor signals lower than VRFTH. If this arrangement is used, the variation in the VDD supply will affect the result.

Enables

Each channel has an enable, ENx. When a channel is disabled its corresponding output is held in the logic 0 state. Also, the outputs are not affected by any changes of signals that may occur on disabled channels. However, when a channel is enabled, the outputs are put into the mode for the length of time as determined by RESET timeout. As noted, when the OVSH is logic 1, the enables of channels 1 and 3 are connected togetherto affect channel 1 output and those for channels 2 and 4 affect channel 2 output. See Figure 4 for timing. The condition whereby all four enables are in the logic 0 state is reserved and should not be used.

Master Reset

The device has a master reset (inverted logic) input, MRB, which provides a means for the system reset to be combined with the voltage supervisor reset functionality. The timing of this input with respect to the RESET/RESETB outputs is shown in Figure 5. Timing specifications are given in the AC Characteristics table. An RC time constant can be associated with this pin to extend the RESET state.

Timing (CDLY, CRESET)

Many of the timing parameters of the device are fixed and listed in the AC Characteristics table. Along with those are the default value for the CDLY function, response time of VOUTx after the corresponding input signal becomes valid, and the C function, defining the timeout until an output is released after an event (an ENx or all enabled VOUTx becoming valid).

CDLY Timing

The delay time (t_{DELAY+}) for each channel is independently adjustable by adding a capacitor to the desired CDLYx pin. The equation that defines the delay is:

$T_{DELAY+} = (Cdly + 18pF) * (V_{TH\_CDLY})/ I_{CH\_CDLY}$

where Cdly is the user chosen, external capacitance connected to CDLY pin, 18pF is the internal capacitance (any significant board capacitance should be added), I_{CH_CDLY} is the charging current with value given in the DC Characteristics table and V_{TH_CDLY} is the threshold voltage utilized by this function, also given in the DC Characteristics table. Note that maximum delay times in this equation are calculated using the minimum charging current and maximum V_{TH} voltage. Minimum delays in the equation are calculated using maximum charging current and minimum V_{TH} voltage.

CRESET Timing

The timeout for the outputs (t_{RP}), when activated by changes of an ENx or VINx signal, is adjustable by the addition of an external capacitor to the CRESET pin. The equation that defines the RESET timeout period is:

t_{RP}=(Creset+ 40pF)*(V_{TH_CRESET}) /I_{CH_RESET}

where Creset is the user chosen, external capacitance, 40pF is the device default and parasitic capacitance (any significant board capacitance should be added), I_{CH_RESET} is the charging current with value given in the DC Characteristics table and V_{TH_CRESET} is the threshold voltage utilized by this function, also given in the DC Characteristics table. Note that maximum delay times in this equation are calculated using the minimum charging current and maximum V_{TH} voltage. Minimum delays in the equation are calculated using maximum charging current and minimum V_{TH} voltage.

Output drive (open drain - power, speed)

The outputs from the device, RESET, RESETB and VOUTx are of the open drain type, having only an active pulldown, with characteristics given in the DC and AC Characteristics tables. Hence, the user must supply an appropriate valued resistor for the pullup. **Note:** This allows for 1) the connecting of several outputs from the given device or other devices and 2) provides for voltage drive-level adjustment by connecting the resistor to an appropriate supply (note the voltage level is constrained by the operating voltage of this device, V_{DD}).

INV function

For further system interface flexibility, the INV pin provides for the logical inversion of the channel 3 and 4 VOUT signals. In all modes, the logic level of the output is inverted from its normal state.

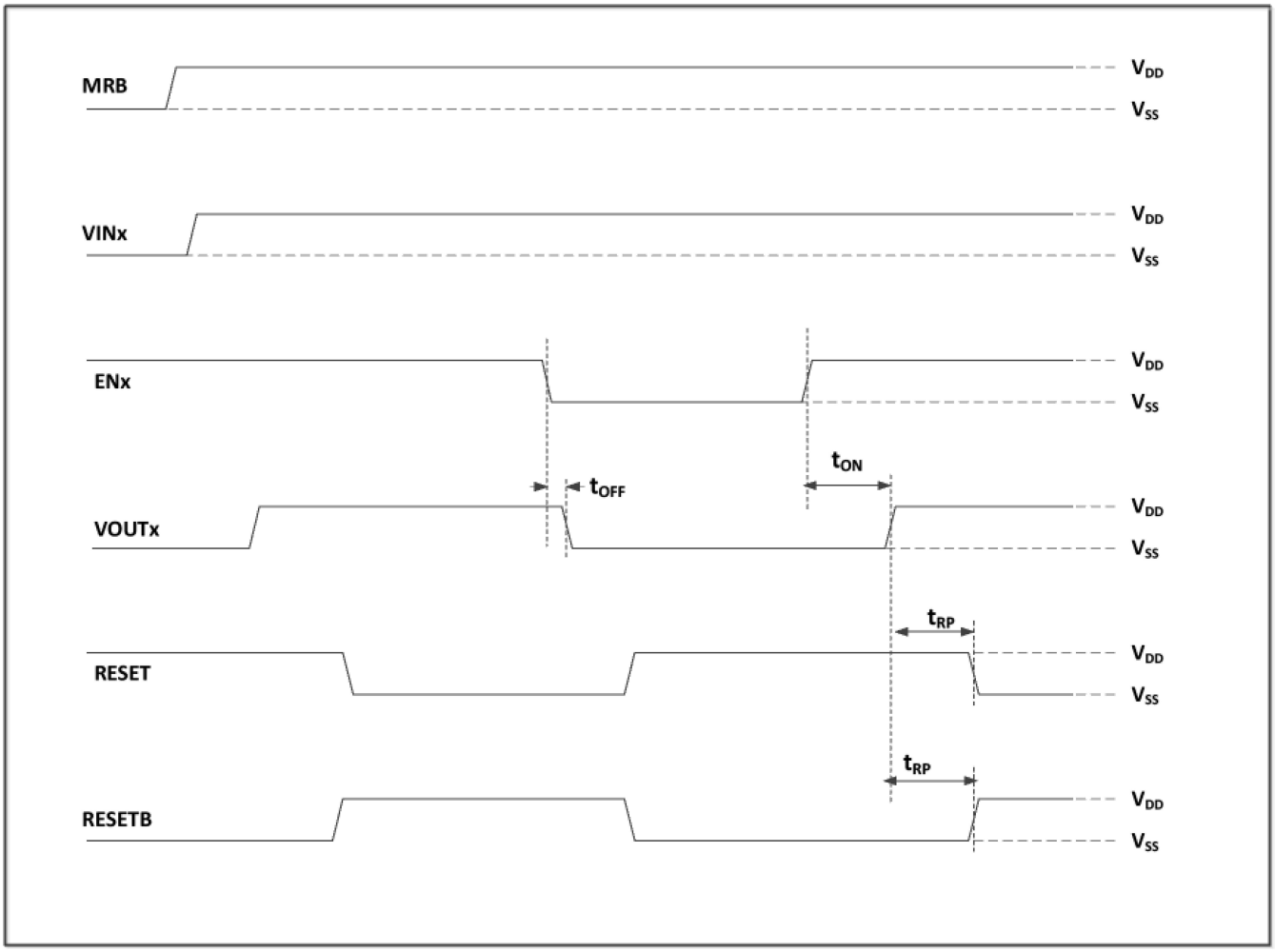


Figure 4. ENx Timing Diagram

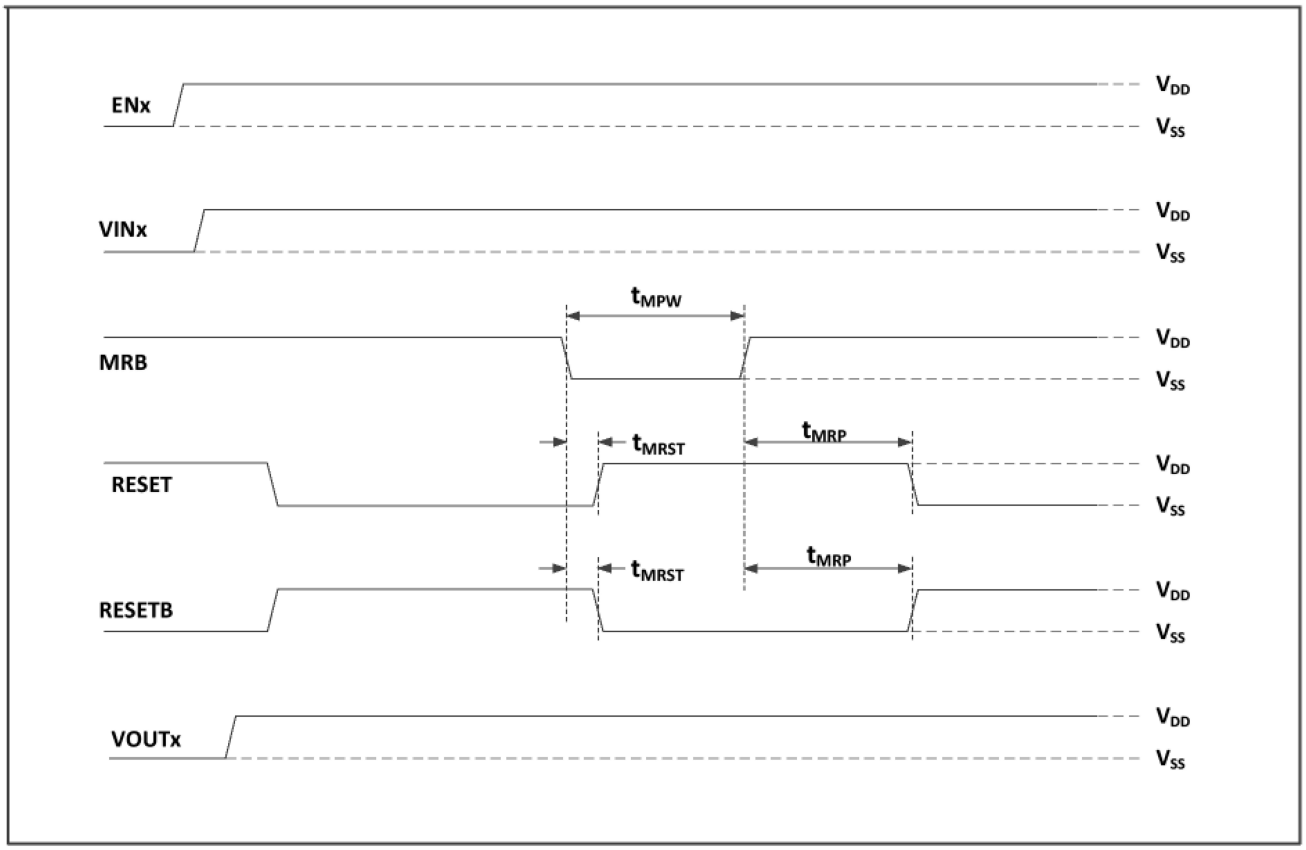


Figure 5. MRB Timing Diagram

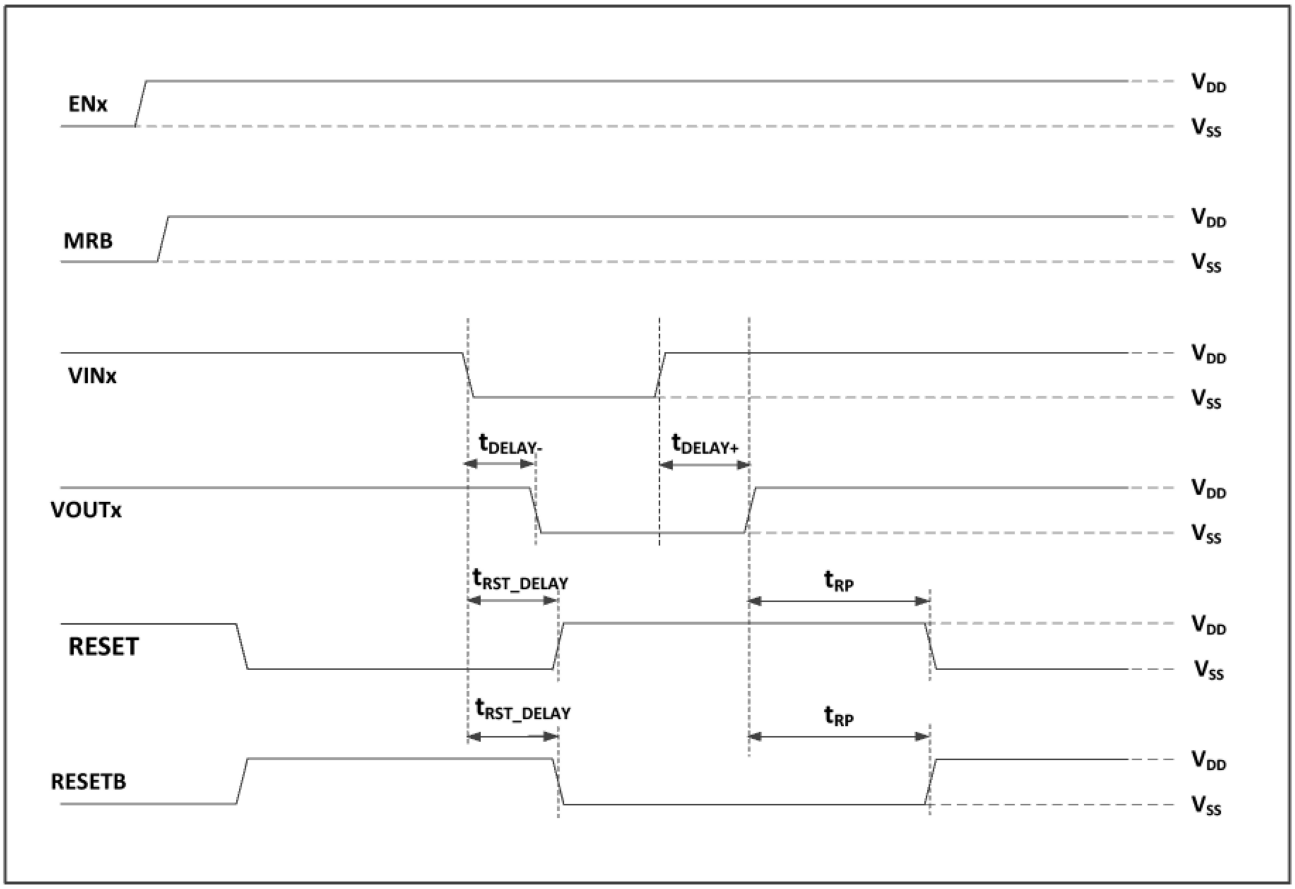


Figure 6. VINx Timing Diagram

Table 1A. Logic Levels for Digital Outputs with Corresponding Digital and Analog Inputs, OVSH=0

ENx	INV	VINx	VOUT1-2	VOUT3-4
0	0	$V_{INx}<V_{TH\_VIN}$	0	0
1	0	$V_{INx}<V_{TH\_VIN}$	0	0
0	0	$V_{INx}>V_{TH\_VIN}$	0	0
1	0	$V_{INx}>V_{TH\_VIN}$	1	1
0	1	$V_{INx}<V_{TH\_VIN}$	0	1
1	1	$V_{INx}<V_{TH\_VIN}$	0	1
0	1	$V_{INx}>V_{TH\_VIN}$	0	1
1	1	$V_{INx}>V_{TH\_VIN}$	1	0

Note:
Effect of INV on VOUT (TOL = x and OVSH = 0), ENx and VINx refer to the corresponding output.

Voltage Supervisor

UT04VS50P

Table 1B. Logic Levels for Digital Outputs with Corresponding Digital and Analog Inputs, OVSH=1

ENx/ENy	INV	VINx/VINy	VOUT1-2	VOUT3-4
0	0	Any V_{INx} and V_{INy}	0	0
1	0	$V_{INx}<V_{TH}$ or $V_{INy}>V_{TH\_OVRV}$	0	0
0	0	Any V_{INx} and V_{INy}	0	0
1	0	$V_{TH}<V_{INx}$ and $V_{INy}<V_{TH\_OVRV}$	1	0
0	1	Any V_{INx} and V_{INy}	0	1
1	1	$V_{INx}<V_{TH}$ or $V_{INy}>V_{TH\_OVRV}$	0	1
0	1	Any V_{INx} and V_{INy}	0	1
1	1	$V_{TH}<V_{INx}$ and $V_{INy}<V_{TH\_OVRV}$	1	1

Notes:

1) Effect of INV on Vout (TOL= x and OVSH=1). ENx/ENy refers to EN1 and EN3 or EN2 and EN4, respectively. VINx/VINy refers to VIN1 and VIN3 or VIN2 and VIN4, respectively. Note: Vout3/Vout4 are not used in this mode.
2) Having all four enables low is an invalid state for the device operation. This state will not cause any harm to the device orsystem, but operation may not be as expected.
3) For OVSH=1, V_{TH_OVRV} is the threshold which is set with external resistors to either the V_{IN3} or V_{IN4} input to monitor an over-voltage condition in conjunction with the under-voltage monitor by VIN1 or VIN2, respectively, as shown in Figure 8 and Figure 9.

Table 2. Quad Input Voltage Threshold Selections

TH1	TH0	VIN1	VIN2	VIN3	VIN4
0	0	3.3	2.5	1.8	1.5
0	1	3.3	1.8	1.5	1.2
1	0	3.3	1.5	1.2	1
1	1	ADJ	ADJ	ADJ	ADJ

Note:
Refer to the section, "Thresholds/Over-Voltage Setting/Tolerance" for information regarding the adjustable threshold.

Table 3: Analog Input Resistance Referenced to V_{SS} (V_{DD} = 4.5V to 5.5V; -55°C < T_C < +125°C)

Analog Input Resistance	Threshold Select		MIN	MAX	Unit
	TH1	TH0			
RIN1	0	0	94	160	kΩ
RIN2	0	0	282	485	kΩ
RIN3	0	0	205	355	kΩ
RIN4	0	0	172	295	kΩ
RIN1	0	1	94	160	kΩ
RIN2	0	1	205	355	kΩ
RIN3	0	1	172	295	kΩ
RIN4	0	1	137	235	kΩ
RIN1	1	0	94	160	kΩ
RIN2	1	0	172	295	kΩ
RIN3	1	0	137	235	kΩ
RIN4	1	0	114	197	kΩ

Note:
Listed in Table 3 are the estimated input resistances, as referenced to V_{SS}, seen at each of the VINx pins. The resistance can be used to estimate the expected load current at that VINx input.

Application Diagrams

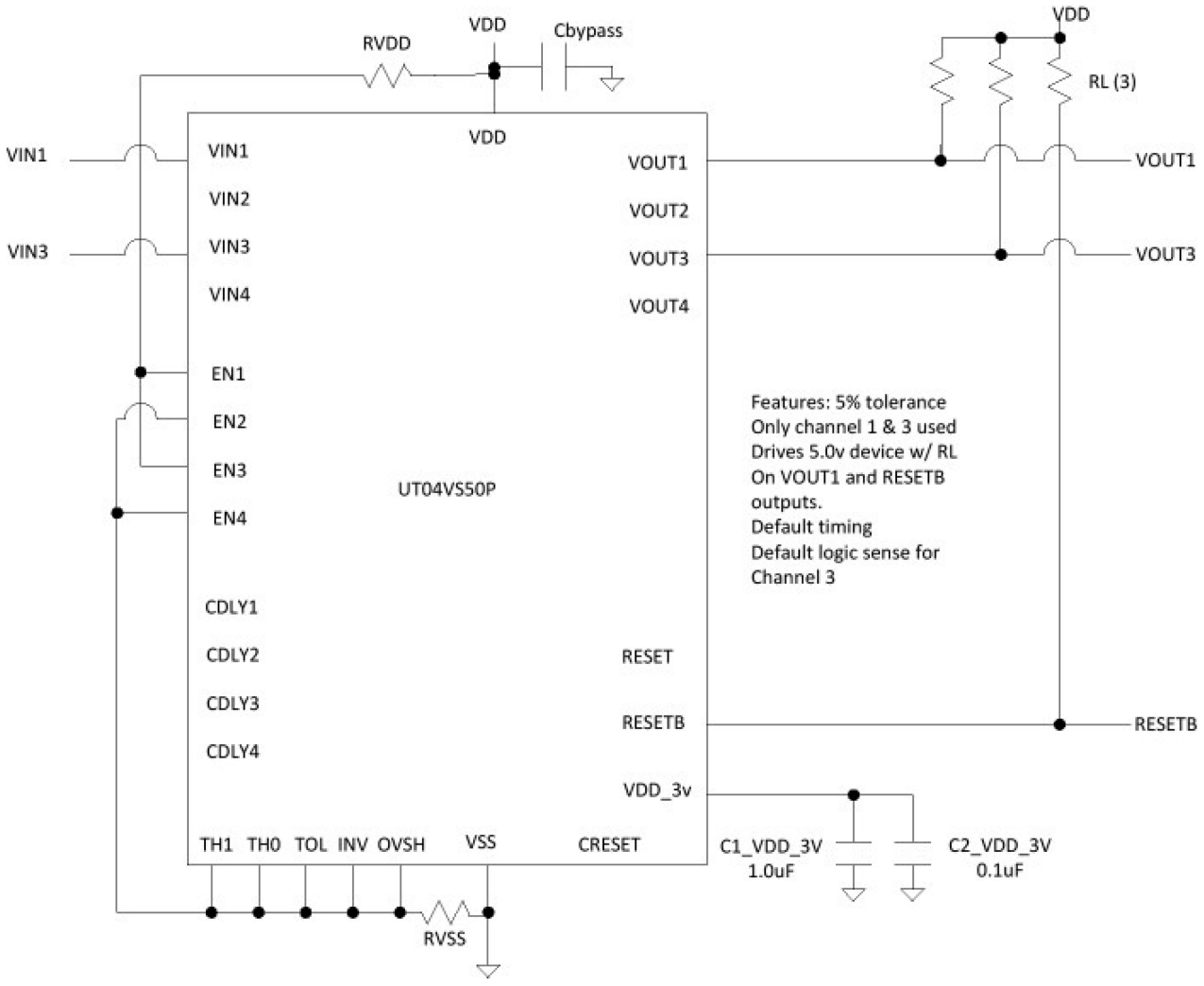


Figure 7. Application example of basic connection

Shown in Figure 7 is a basic application with pullup resistors on VOUTx and RESETB. Inputs INV, MRB, TH0, TH1, TOL, OVSH and ENx are tied to appropriate signals or supplies. VINx are hooked to supplies that are to be monitored and supply is connected. Letting CDLYx and CRESET float, sets the associated delays at their default value.

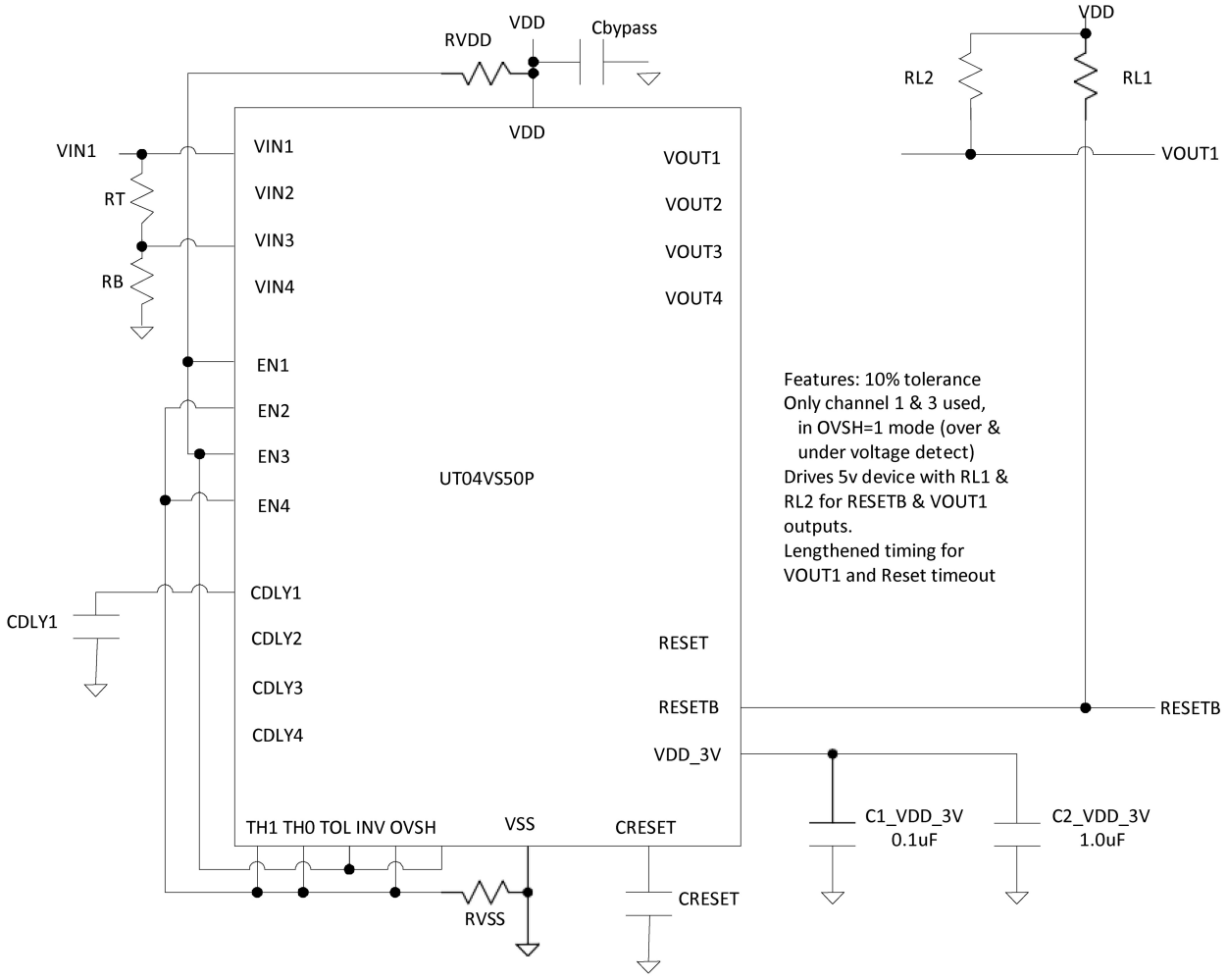


Figure 8. Extended use application showing OVSH connection for channel 1

Shown in Figure 8 is an extended application showing the use of Cdly and Creset capacitors. OVSH is set to logic 1 to highlight the under- and over-voltage detection mode connections. Thus, a resistor voltager-divider on channel 3 is connected from the channel 1 source.

Voltage Supervisor

UT04VS50P

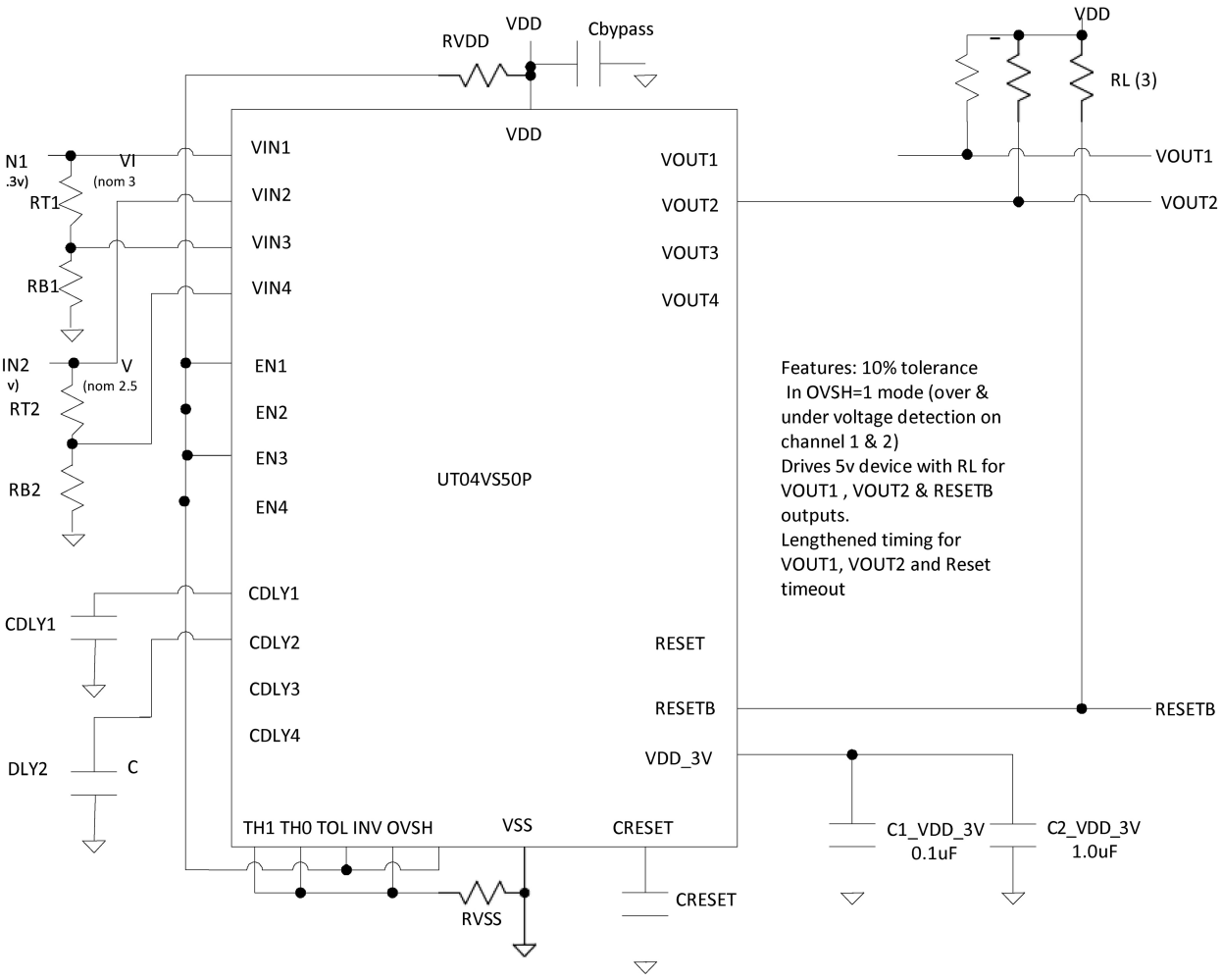


Figure 9. Extended use application showing OVSH connection for channel 1 and 2

Shown in Figure 9 is an extended application showing the use of Cdly and Creset capacitors. OVSH is set to logic 1 to highlight the under- and over-detection mode connections on channel 1 and channel 2. Thus an resistor voltage dividers on channel 3 and 4 are connected from the channel 1 and 2 source, respectively.

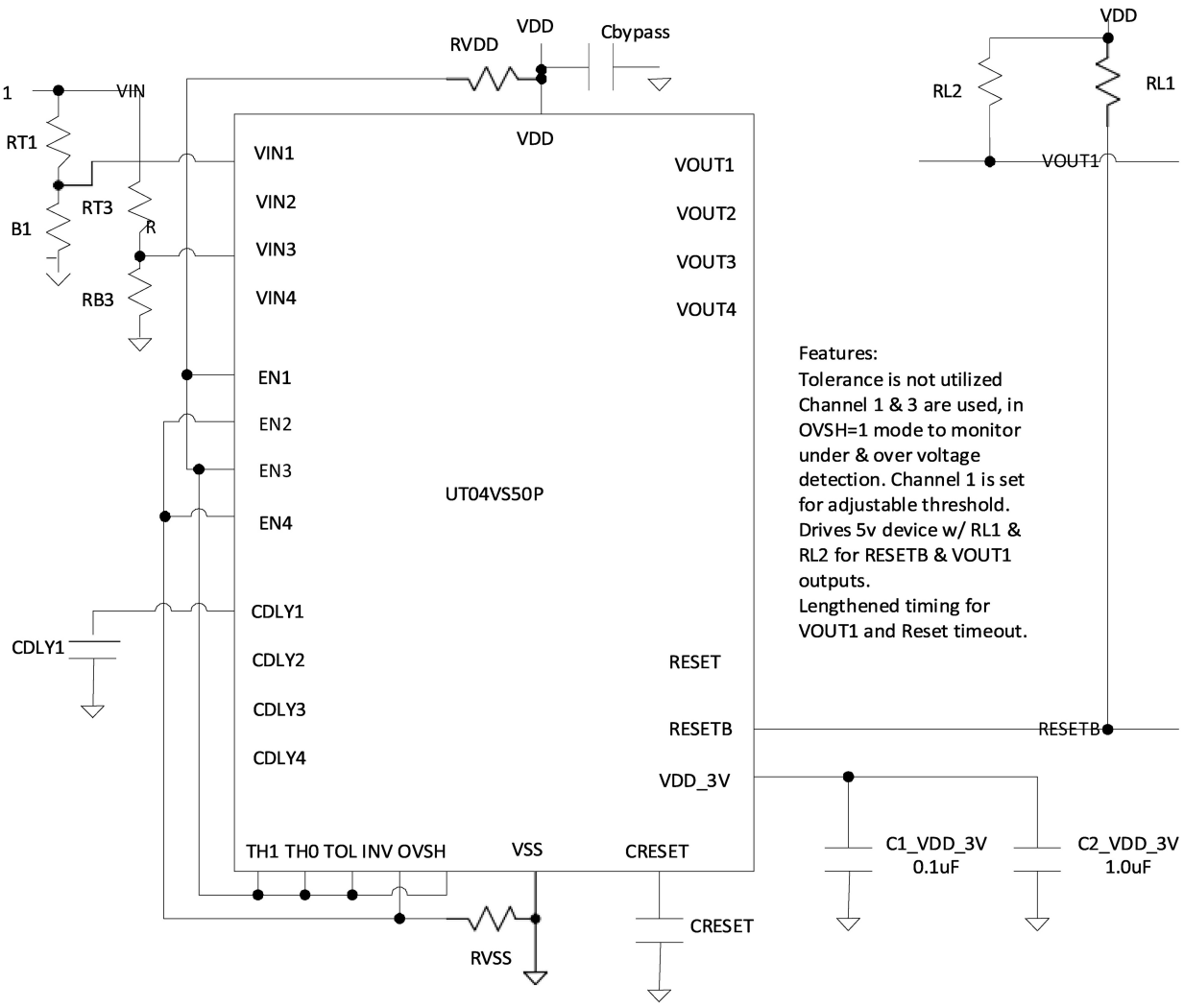


Figure 10. Extended use application showing OVSH connection for channel 1 and 3 for adjustable threshold

Shown in Figure 10 is an extended application showing the use of Cdly and Creset capacitors. OVSH is set to logic 1 to highlight the under and over-voltage detection mode connections with adjustable threshold on channel 1. Two resistor voltage dividers will be used for channel 1and 3. The resistor voltage divider (RT1, RB1) on channel 1 sets the threshold under-voltage monitor. The resistor voltage divider (RT3, RB3) is connected from the channel 1 source to channel 3 to monitor over-voltage on source 1

UT04VS50P

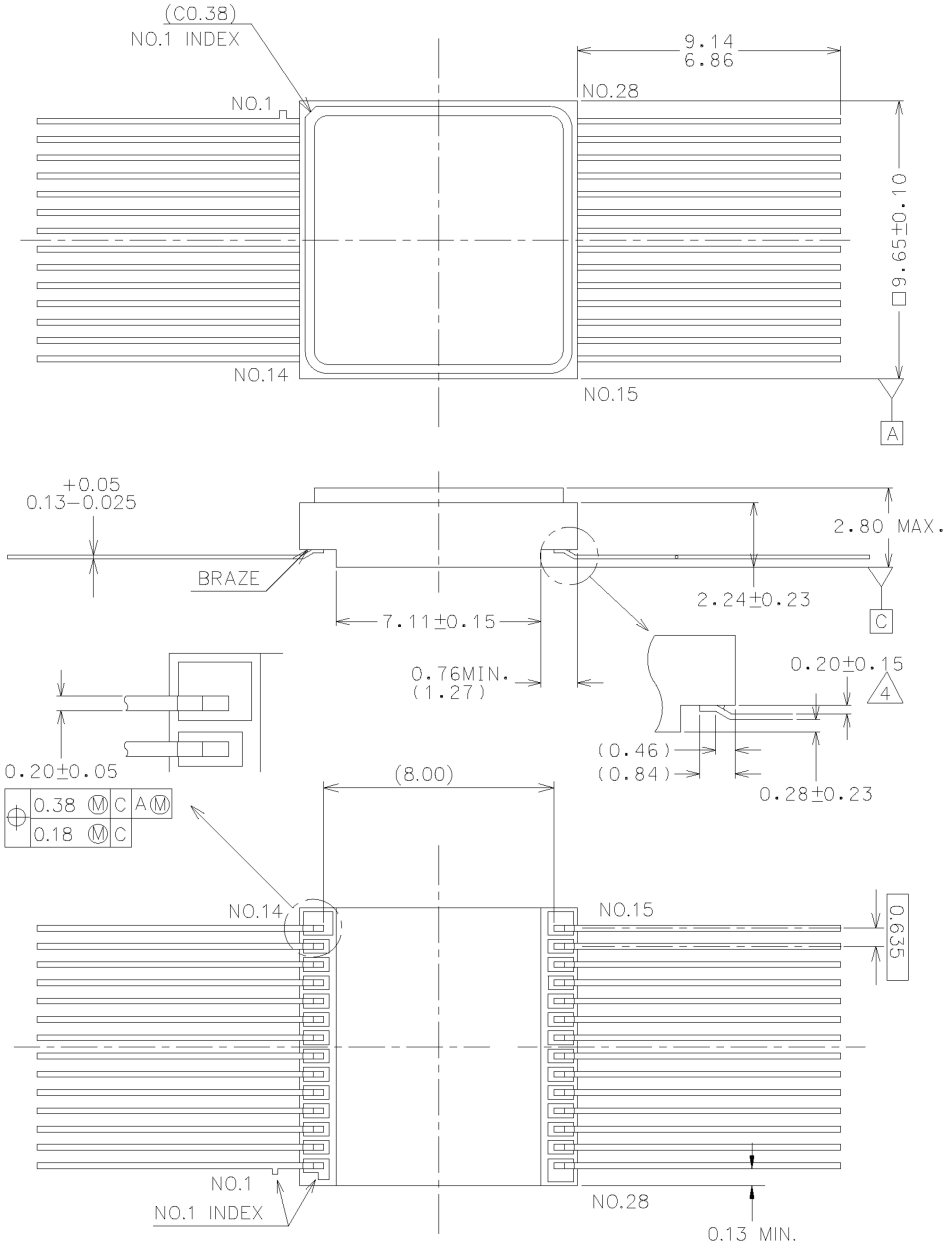


Figure 11. 28-pin Flatpack

Notes:

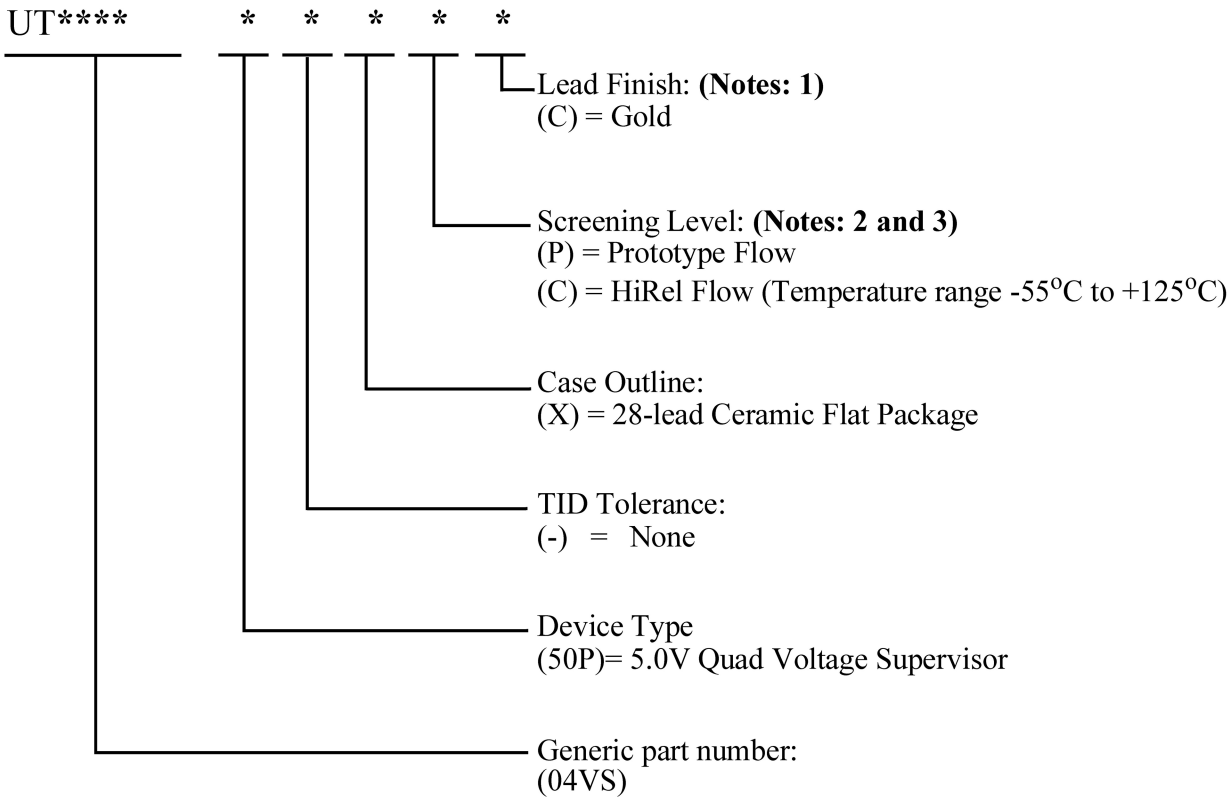
1) Package Material: Opaque 90% Minimum Alumina Ceramic.
2) All Exposed Metal Areas Are Gold Plated 100 To 225 Microinches Thick Over Electroplated Nickel Undercoating 100 To 350 Microinches Thick Per MIL-PRF-38535.
3) The Seal Ring Is Electrically Connected to VSS.
4) Dogleg Geometries Optional Within Dimensions Shown.

Voltage Supervisor

UT04VS50P

Ordering Information

UT04VS50P Voltage Supervisor



Notes:

1) Lead finish is "C" (Gold) only.
2) Prototype flow per CAES Manufacturing Flows Document. Devices are tested at 25°C only. Radiation neither tested nor guaranteed.
3) HiRel Flow per CAES Manufacturing Flows Document. Radiation neither tested nor guaranteed.

Voltage Supervisor

UT04VS50P

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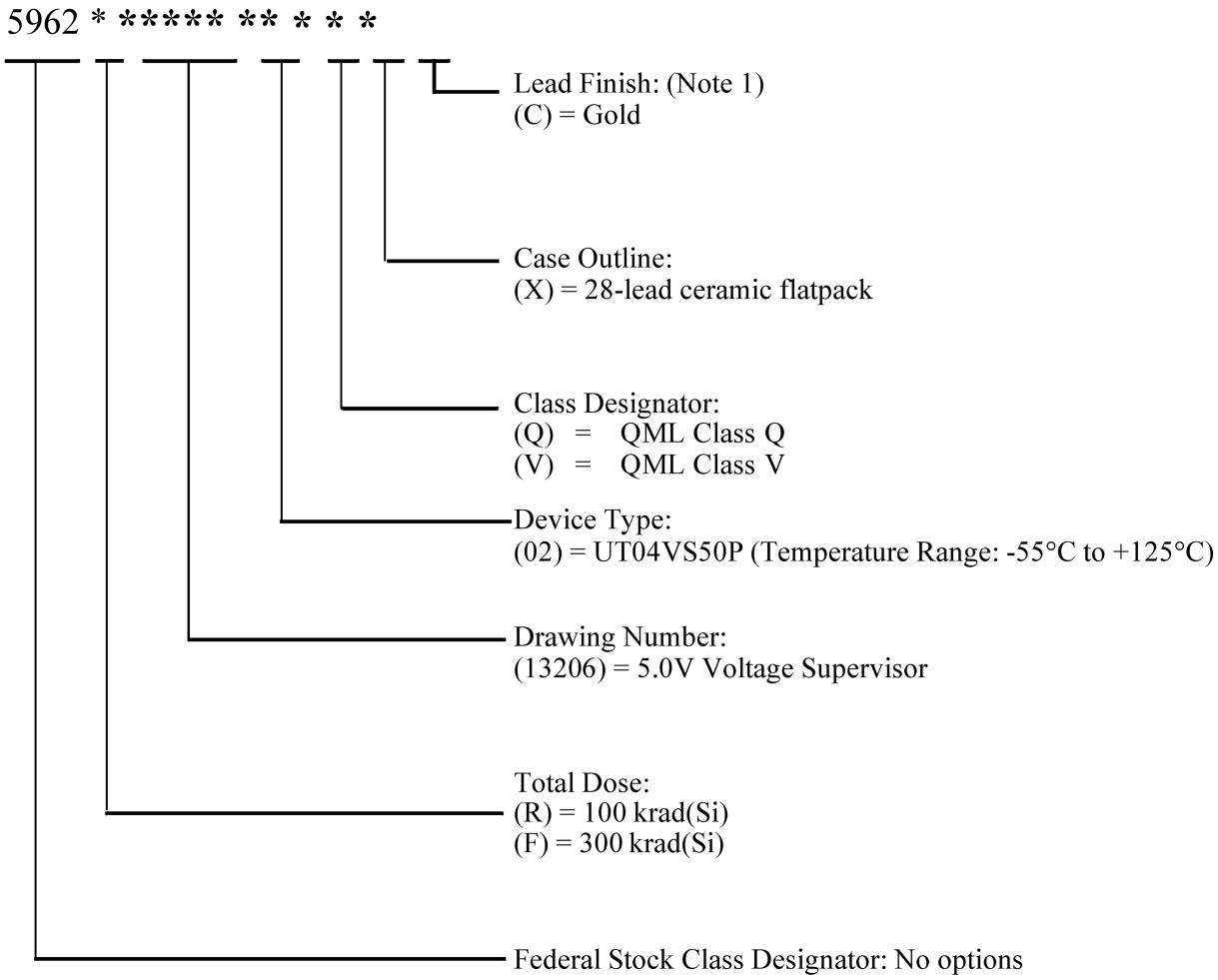

Note:

1) Lead finish is "C" (Gold) only.

DATASHEET

RELEASED 7/31/20

Voltage Supervisor

UT04VS50P

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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